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SCOPE

The purpose of this workshop is to bring researchers and practitioners of LSI testing from all over the world together to exchange ideas and experiences in register transfer level (RTL), high level and system level testing. WRTL T'16, the seventeenth workshop, will be held in conjunction with the 25th Asian Test Symposium (ATS'16) in Hiroshima, Japan. We hope and expect this workshop provides an ideal forum for frank discussion on this important topic for the future system-on-a-chip (SoC) devices.

Areas of interest include but not limited to:

- RTL fault modeling, ATPG, DFT, BIST
- High-level fault modeling, testing and synthesis for testability
- Functional fault modeling and test bench generation
- 3D IC testing
- SoC/NoC testing, test scheduling, core-based testing, interconnect testing
- Reliable SoC, system level reliability, self repair, fault tolerant SoC
- Microprocessor testing, design verification

SUBMISSIONS

Authors are invited to submit paper proposals for presentation at the workshop. The proposal may be an extended summary (up to 1,000 words) or a full paper (4-6 pages) and should include: title, full name and affiliation of all authors, abstract, keywords and the name of contact author.

KEY DATES

Submission deadline: August 19, 2016

Notification: September 25, 2016

Camera ready due: October 10, 2016

FURTHER INFORMATION

Web Site: <http://www.ieee-wrtlt.org/2016/>

General Information:

Michiko Inoue, NAIST, Japan,
kounoe[AT]is.naist.jp

Program Related Information:

Hiroyuki Yotsuyanagi, Tokushima U. Japan,
yanagi4[AT]ee.tokushima-u.ac.jp
Xiaoqing Wen, Kyushu Institute of Technology, Japan,
Wen[AT]cse.kyutech.ac.jp

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