

WRTL T'16

CALL FOR PARTICIPATION

The Seventeenth Workshop on RTL and High Level Testing

November 24-25, 2016, Aki Grand Hotel, Hiroshima, JAPAN

In conjunction with the 25th Asian Test Symposium (ATS'16)

<http://www.ieee-wrtl.org/2016/>

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SCOPE

The purpose of this workshop is to bring researchers and practitioners of LSI testing from all over the world together to exchange ideas and experiences in register transfer level (RTL), high level and system level testing. WRTL T'16, the seventeenth workshop, will be held in conjunction with the 25th Asian Test Symposium (ATS'16) in Hiroshima, Japan. We hope and expect this workshop provides an ideal forum for frank discussion on this important topic for the future system-on-a-chip (SoC) devices.

Areas of interest include but not limited to:

- RTL fault modeling, ATPG, DFT, BIST
- High-level fault modeling, testing and synthesis for testability
- Functional fault modeling and test bench generation
- 3D IC testing
- SoC/NoC testing, test scheduling, core-based testing, interconnect testing
- Reliable SoC, system level reliability, self repair, fault tolerant SoC
- Microprocessor testing, design verification

VENUE

WRTL T'16 will be held at Aki Grand Hotel that is placed just in front of Miyajima Island. It takes around 40 minutes by train from Hiroshima City. Miyajima (Itsukushima Shinto Shrine) is registered as a UNESCO World Heritage along with Hiroshima Peace Memorial (Genbaku Dome) at Hiroshima City which is a venue of ATS'16. You can enjoy a scenery of Miyajima including Itsukushima Shrine beyond Seto Inland Sea from Aki Grand Hotel.

Tour to Miyajima (Optional)

You can visit Itsukushima Shrine in Miyajima island in the early morning on November 25. The Workshop will provide a boat to Miyajima directly from the pier of the hotel at 6:00 a.m. (The number of participants will be limited)

Advanced Program Overview

WRTL T2016 starts with Welcome Lunch at Aki Grand Hotel and includes keynote speech, invited talk, and Banquet (Nov.24), and optional tour to Miyajima, invited talk, and panel session (Nov.25), along with technical sessions.

Keynote Speech (Nov.24)

Prof. Matteo Sonza Reorda (Politecnico di Torino, Italy)

Invited Talk (Nov.24)

Prof. Adit D. Singh (Auburn University, USA)

“Why Open Defects Should be Explicitly Targeted During Test”

Invited Talk (Nov.25)

Prof. Hans-Joachim Wunderlich (U. of Stuttgart, Germany)

“Multi-Level High-Throughput Simulation for Design & Test Validation”

Early bird Registration Deadline: Mon Oct.17, 2016 <http://www.ieee-wrtl.org/2016/>

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