WRTLT'12 Advance Program

November 22, 2012

13:25 – 14:25
Plenary Session 1
Keynote Address
Hardware Trojan Detection at High Level
R. S. Chakraborty (Indian Institute of Technology, Kharagpur)
Invited Talk (1)
TRUDEVICE: a COST Action in Europe
I. Polian (University of Passau)

14:30 – 15:20
Session 1 High Level Testing & Secure Testing
1.1 Generating Directed Tests for C Programs using RTL ATPG
J. Raik, T. Drenkhan, M. Jenihhin, T. Viilukas, A. Karputkin, A. Chepurov R. Ubar (Tallinn University of Technology)
1.2 WAGSR: Web Application for Generalized Feed Forward Shift Registers (short)
K. Fujiwara (Akita University), H. Fujiwara (Osaka Gakuin University)
1.3 An Estimation of Trojan Circuits on AES Encryption Circuits (short)
M. Yoshimura (Kyushu University), A. Ogita, T. Hosokawa (Nihon University)

15:35 – 16:55
Session 2 Test Generation & Design for Testability
2.1 On detectability analysis of open faults using SAT-based test pattern generation considering adjacent lines
J. Yamashita, H. Yotsuyanagi, M. Hashizume (University of Tokushima), K. Kinoshita (Osaka Gakuin University)
2.2 Increasing Test Compaction Abilities of SAT-based ATPG through Fault Detection Constraints
S. Eggersglüß (DFKI), M. Diepenbeck, R. Wille (University of Bremen), R. Drechsler (DFKI)
2.3 Estimating the Number of Don't-Care Bits in Test Vectors
K. Miyase, S. Kajihara, X. Wen (Kyushu Institute of Technology)
2.4 A Test Point Insertion Method Using Don’t Care Identification and Test Compaction Techniques to Reduce Test Application Time for Transition Faults
T. Hosokawa, A. Takahashi, H. Yamazaki (Nihon University), M. Yoshimura (Kyushu University)

17:00 – 18:15

Session 3 Reliability & Dependable SoC

3.1 Which Metric is Better for Quantification of Hardware Faults-induced Errors?
Y. Fang, H. Li, X. Li (Chinese Academy of Sciences)
3.2 A Realization Method of Fast and Dependable Programmable Logic Controllers
R. Kawaguchi, Y. Yamada, K. Takahashi, Y. Urano, Y. Iguchi (Meiji University)
3.3 An Efficient Fault Simulation Algorithm for Analyzing Incorrect State Transitions Induced by Soft Errors in Sequential Circuits
T. Takata, M. Yoshimura, Y. Matsunaga (Kyushu University)
3.4 A Study on Error Correctable Test Pattern Generator for Reliable Built-in Self Test (short)
Y. Fukazawa, T. Iwagaki, H. Ichihara, T. Inoue (Hiroshima City University)

November 23, 2012

9:00 – 10:10

Plenary Session 2

Invited Talk (2)

The Past and Future of WRTLT
Y. Min (Chinese Academy of Sciences), H. Fujiwara (Osaka Gakuin University)

Invited Talk (3)

System Level Testing Considerations as we Move from RTL to ESL
Zainalabedin Navabi (University of Tehran)

10:25 – 11:40

Session 4 Delay Testing

4.1 Capturing Post-Silicon Variations by Layout-Aware Path-Delay Testing
X. Zhang, J. Ye, Y. Hu, X. Li (Chinese Academy of Science)
4.2 Exact and Heuristic Methods of Generating Compact Tests for Hold-time Violations
T. Iwagaki, H. Ichihara, T. Inoue (Hiroshima City University), K. K. Saluja (University of Wisconsin-Madison)
4.3 A Reduction Technique of Volume of Input Sequences for Time-Multiplexed Delay Measurement Using Embedded Delay Measurement Circuit
K. Katoh, S. Hoshina Tsuruoka (Tsuruoka National College of Technology), K. Itagaki (Nagaoka University of Technology)
4.4 Delay measurement of global routing resources in FPGA for small delay defect detection (short)
Kazuteru Namba, Nobuhide Takashina, Hideo Ito (Chiba University)

13:10 – 14:20

Panel Session

Theme: "Can RTL test techniques be applied to software?"

Coordinator: J. Raik (Tallinn University of Technology)

Panelists:

Dr. Görschwin Fey, Bremen University/ German Institute for Aerospace DLR, Germany

Prof. Masahiro Fujita, University of Tokyo, Japan

Prof. Zainalabedin Navabi, University of Tehran, Iran/ Worcester Polytechnic Institute, US

Prof. Huawei Li, Institute of Computing Technology, Chinese Academy of Sciences, China

14:25 – 15:40

Session 5 Low Power Testing & Random Testing & Online Testing

5.1 Analysis on the Effect of Distance Hypothesis in Anti-Random Testing

S. Gu, S. Xu, Y. Wu (Shanghai University)

5.2 Power Aware Scan Flip Flop Design for Scan Test

S. Ahlawat (Indian Institute of Technology, Bombay), A. K. Suhag (Gautam Buddha University), J. T. Tudu (Indian Institute of Science, Bangalore), V. Singh (Indian Institute of Technology, Bombay)

5.3 An Improved Method of Per-Cell Dynamic IR-Drop Estimation Based on the Weighted Switching Activity Metric

Y. Yamato, Y. Akiyoshi, T. Yoneda, K. Hatayama, M. Inoue (NAIST)

5.4 An Online Method for Serial Interconnects Testing (short)

S. S.-Kohan, S. Keshavarz, Z. Navabi (University of Tehran)

16:10 – 17:15

Session 6 SoC/NoC Testing & 3D IC Testing

6.1 Output Voltage Estimation Method of Hard Open TSV in 3D ICs

M. Hashizume, S. Kondo, E. Haraguchi, H. Yotsuyanagi (University of Tokushima), T. Tada (Tokushima Bunri University), Z. Roth (Florida Atlantic University)

6.2 A Cost-Effective Scheme for 3-D Stacked NoC Router and Interconnect Testing (short)

D. Xiang (Tsinghua University)

6.3 On Automating The IEEE 1500 Core Wrapper Insertion for SOC Testing (short)

M. I. M. Ibrahim, F. A. Hussin (Universiti Teknologi PETRONAS)

6.4 An Algorithm for Core-Based Test Time Optimization for 3-D Integrated Circuits (short)

M. Pradhan (Jadavpur University), C. Giri, H. Rahaman (Bengal Engineering and Science University, Shibpur) , D. K. Das (Jadavpur University)