



# IEEE WRTL'14 Call For Papers

The Fifteenth Workshop on RTL and High Level Testing

Hangzhou, China, Nov.19-20, 2014

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## Important Dates

Submission Deadline: *Aug. 15, 2014*

Acceptance Notification: *Sep. 22, 2014*

Camera Ready: *Oct. 10, 2014*

## Further Information

Email: [wrtl14@ict.ac.cn](mailto:wrtl14@ict.ac.cn)

URL: <http://wrtl2014.ict.ac.cn>



## Scope

The purpose of this workshop is to bring researchers and practitioners on LSI testing from all over the world together to exchange ideas and experiences on register transfer level (RTL) and high level testing.

WRTL'14, the fifteenth workshop, will be held in conjunction with the 23rd Asian Test Symposium (ATS) in Hangzhou, China. We expect this workshop to provide an ideal forum for interactive discussion on important topics of future system-on-a-chip (SoC), 3D ICs. Areas of interest include but are not limited to:

- RTL fault modeling, ATPG, DFT, BIST
- High-level/behavior fault modeling, testing and synthesis for testability
- Functional fault modeling and test bench generation
- 3D IC testing
- SoC/NoC testing, test scheduling, core-based testing, interconnect testing
- Reliable SoC : system level reliability, self repair, fault tolerant SoC
- Microprocessor testing , design verification
- Low power testing
- Test compression, ATPG, DFT, BIST
- Hardware trojan detection, secure testing

## Submissions

Authors are invited to submit paper proposals for presentation at the workshop. The proposal may be an extended summary (1,000 words) or a full paper (4-6 pages, two columns). The submission should include: title, full name and affiliation of all authors, 50 words abstract, keywords and the name of contact author, in a standard IEEE two-column format. The submission will be considered evidence that upon acceptance the author(s) will present the paper at the workshop. Digest of Papers will be handed out at the workshop.

## Sponsored by

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