

The 22nd IEEE Workshop on RTL and High Level Testing



WRTLTL 2021

November 25-26, 2021

Virtual Workshop

Call for Papers

The purpose of this workshop is to bring researchers and practitioners of LSI testing from all over the world together (using tools for on-line interaction) to exchange ideas and experiences in register transfer level (RTL), high level and system level testing. WRTLTL 2021, the twenty-second workshop, will be held immediately after the 30th Asian Test Symposium (ATS 2021) as a virtual event. The workshop aims to encourage the presentation and discussion of truly innovative and "out-of-the-box" ideas aimed at addressing the challenges of high level test. We hope and expect this workshop will provide an ideal forum for discussion on this important topic for future system-on-a-chip (SoC) devices.

Scope

Areas of interest include but are not limited to:

- RTL fault modeling, ATPG, DFT, BIST
- High-level fault modeling, testing and synthesis for testability
- Functional fault modeling and test bench generation
- System Level Testing
- 3D IC testing
- SoC/NoC testing, test scheduling, core-based testing, interconnect testing
- Reliable SoC, system level reliability, self-repair, fault tolerant SoC
- Microprocessor testing, design verification
- Low power testing and Test compression
- Hardware trojan detection and secure testing

Submissions

Authors are invited to submit paper proposals for presentation at the workshop. The proposal may be an extended summary (1,000 words) or a full paper (4-6 pages, two columns). The submission should include title, full name, and affiliation of all authors, 50 words abstract, keywords and the name of contact author, in a standard IEEE two-column format. All submissions are now to be made electronically. Digest of Papers will be handed out to the workshop participants.

Key Dates

Submission deadline: **August 20, 2021**

Notification of acceptance: **September 24, 2021**

Camera-ready: **October 29, 2021**

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